Silicon Strip Detectors with Custom VLSI Readout Electronics for the SIS Instrument on ACE

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ABSTRACT

We discuss the design and implementation of the trajectory system for the Solar Isotope Spectrometer (SIS) instrument on the Advanced Composition Explorer (ACE) mission. Thin, large area silicon strip detectors instrumented with a custom very large scale integrated circuit (VLSI) pulse height analyzer (PHA) for each strip are used to simultaneously achieve large geometrical factor and the capability for making precise measurements in even the largest solar energetic particle (SEP) events.

INTRODUCTION

SIS is designed to measure the isotopic composition of heavy elements in SEP events and anomalous cosmic rays. This is accomplished using a stack of silicon solid state detectors to make redundant measurements of energy loss and total energy, together with a trajectory system for determining the position and angle at which each particle penetrates the instrument. The trajectory system must provide low threshold energy, large geometrical factor, high count rate capability, and good spatial and energy resolution. This is accomplished through the use of thin, two-dimensional position sensitive silicon detectors ("matrix" detectors) instrumented with separate pulse height analyzers for each of 64 x strips and 64 y strips per detector. The detectors and the custom VLSI circuitry used to process their signals were specially developed for the ACE mission.

SILICON MATRIX DETECTORS

The first two detectors penetrated by a particle entering the SIS instrument are matrix detectors (Figure 1) designed to provide both trajectory and energy loss information. The active area of each matrix detector is a 34 cm^2 octagon segmented into 64 strips with a 1 mm pitch on each surface, and having front- and back-surface strips oriented at 90° to one another. These ion-implanted detectors were produced for SIS by Micron Semiconductor Ltd. in thicknesses ranging from 50 to 90 μm. A detailed discussion of the design and testing of these devices has been given by Wiedenbeck et al. (1996).

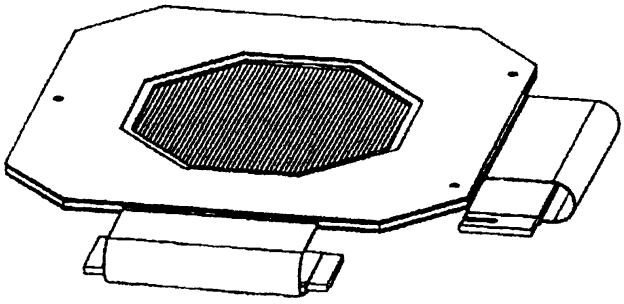

Fig. 1: SIS matrix detector. The thin (~ 70 μm) silicon detector is bonded into a G-10 mount with flexible connections to the circuit board containing the readout electronics.

The thin silicon wafers are bonded into a G-10 detector mount with a silicone resin. Redundant sets of aluminum wire bonds are used to connect the aluminum strip contacts on the detector to corresponding gold-plated copper pads on the mount. The detector signals are connected through copper traces on a kapton "flex-strip" to a rigid G-10 connector designed to mate with a high density connector on the board containing the matrix detector PHA electronics.

VLSI PULSE HEIGHT ANALYZERS

Figure 2 is a block diagram of one PHA. A matrix detector strip is DC coupled to the input of the charge sensitive amplifier (CSA). The output voltage of a precision, unity-gain buffer which follows the CSA is used to charge one of three hold capacitors (C1 through C3) selected by externally controlled switches. Under quiescent conditions when no detector pulse is present, the CSA signal is switched between C2 and C3 every 3 μsec. Thus one of these capacitors is charging while the other holds a steady sample of the baseline (which changes slowly over time due to unbalanced DC current being integrated by the CSA, see below). When a heavy nucleus passes through the detector the ionization charge it produces is integrated by the CSA causing its output to step up (time constant $\sim$ 100 nsec) from the present baseline by an amount proportional to the collected charge. Under the control of external logic, switch SW1 is closed causing capacitor C1 to charge to the final voltage reached by the CSA output. At the same time the alternate sampling of the baseline onto C2 and C3 is halted and the capacitor with the most recent good sample is connected to the reference input of a comparator. A DC current source causes the voltage on C1 to linearly ramp down until it reaches the stored baseline voltage. The output of the Wilkinson comparator is then a logic pulse with width proportional to the detected ionization charge. To ensure that the "rundown" time is non-zero even for very small input signals, a constant pedestal voltage is applied via C4 before beginning the ramp. At the end of the rundown interval the state of a counter running at 8 MHz is latched to give a 12-bit digitized representation of the pulse height.

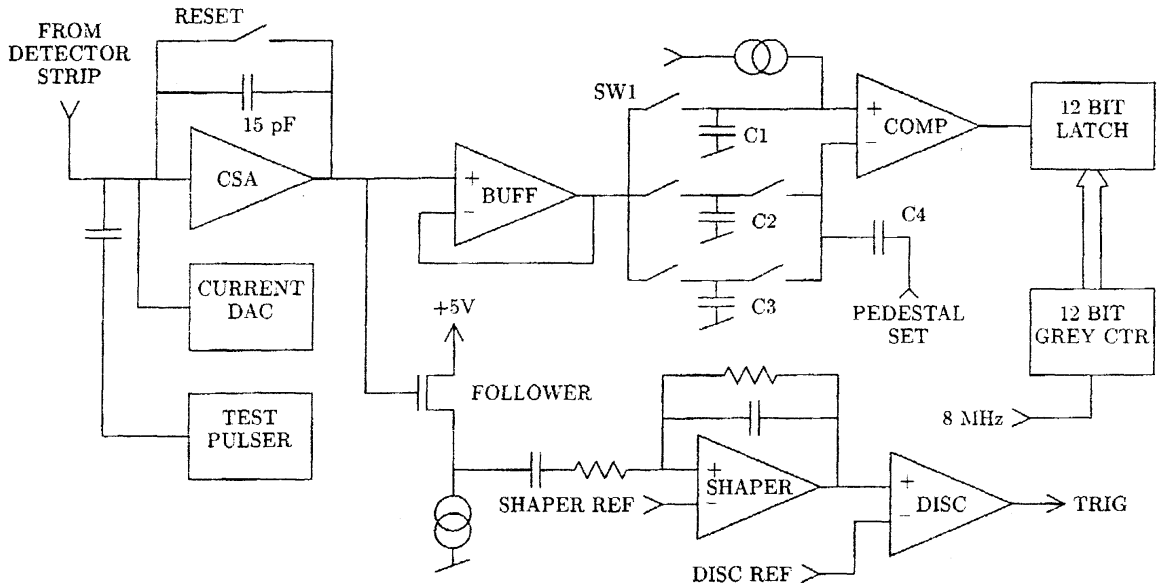

Fig. 2: Block diagram of one of 16 PHAs on a matrix VLSI chip. A single grey code counter serves all 16 PHA channels on the chip. This circuit has been discussed by Cook et al. (1993).

A second branch of the circuit is used to produce discriminator signals which can be used as inputs to external control logic. The CSA output is processed by a source follower and a shaping amplifier with a peaking time $\sim$ 500 nsec. Two discriminators (one of which is shown in Figure 2) compare the shaped pulse with externally provided reference voltages (typically set to correspond to $\sim$ 3.5 and $\sim$ 16 MeV from the detector) and produce logic pulses for signals above these thresholds.

After an event has been processed, an externally-controlled reset switch is closed to discharge the integration capacitor. Because the CSA input is DC coupled to the detector strip, it integrates the

strip's DC leakage current as well as the signal charge. The CSA reset switch must be periodically closed to clear this charge from the capacitor. In order to keep this reset interval relatively long (milliseconds) a current-output digital-to-analog converter (IDAC) is provided to add a programmable current to cancel the leakage current to within $\sim 2\,\mathrm{nA}$. Under external control the CSA can be allowed to integrate for an extended time ($\sim 500\,\mu\mathrm{sec}$) to obtain a precise measurement of the residual unbalanced current. This value is then used as the basis for updating the IDAC setting. In SIS this leakage current balancing is performed every 512 seconds. The IDAC settings are read out as part of the instrument's housekeeping data, allowing us to track the leakage current on each strip and monitor the health of the detector. Similarly, pedestals are monitored by periodically triggering a conversion when no input signal is present.

A CMOS VLSI chip has been developed which contains 16 of the matrix detector PHA circuits. Thus the processing of signals from the 128 strips on each matrix detector requires a total of 8 of these chips. The circuit can be configured to handle either positive or negative charge inputs, so the same type of devices can be used to process signals from both detector surfaces. Flight chips were fabricated using a radiation hard $1.2\,\mu\mathrm{m}$ process by UTMC.

For the chips containing 16 PHAs a number of signals have been made common to all channels in order to reduce the complexity of the interfaces to external circuitry. These include the switch controls for the sample-and-hold and the CSA reset, the start of the rundown interval, the injection of the pedestal signal, and the triggering of the test pulser. A logical OR is formed of the 16 discriminator outputs to produce a single trigger signal which is brought out for use by external control logic. The OR of the 16 Wilkinson comparator signals is also brought off-chip to indicate when all conversions are complete and to provide a relatively prompt indication of the size of the largest detected signal.

Each PHA has an on-chip test pulser. The analog DC reference for this pulser and the logic signal used to trigger a pulse are common to all 16 channels. Similarly, all channels share common discriminator reference voltages.

Table 1. Matrix VLSI Characteristics

Parameter	Value
PHAs per chip	16
power per PHA	13 mW
full scale signal	31 pC (700 MeV Si)
dynamic range (full scale:threshold)	1400:1
gain variation	$\lesssim 10\%$ [1]
threshold variation	$\sim 10\%$ rms at 3 MeV
ADC type	12-bit Wilkinson
dead time per event	$(\sim 6 + 0.125\,N)\,\mu\mathrm{sec}$ [2]
integral nonlinearity (+ input)	$\sim 1\%$ of full scale
integral nonlinearity (− input)	$\sim 0.1\%$ of full scale
max. leakage current cancellation	$1\,\mu\mathrm{A}$
chip size	$(13.5\,\mathrm{mm})^2$, 84 pins
temp. coef. of gain	$< \pm 20$ ppm/C
offset temp. variation (−20C to 40C)	< 1 chan (after correction)
cross talk for full scale pulse	2 chan

[1] among channels on one chip. Chip-to-chip variations can be larger.
[2] N = pulse height channel number, including pedestal.

The IDACs used for leakage current compensation are separate for each of the channels, but the digital control inputs for all 16 IDACs are serially loaded through a single input. This serial

command loop is also used to load other configuration bits, including masks which can be used to remove selected PHAs from the ORs of the trigger and ADC comparator signals. This feature is useful for disabling strips which are generating excessive noise. Another serial connection is used for reading out the digitized pulse heights from all 16 PHAs.

Table 1 summarizes some important characteristics of the matrix VLSI circuits.

CALIBRATION

In order to obtain pulse height information from the matrix detectors with sufficient precision for isotope identification (few tenths of a percent) it is necessary to correct for strip-to-strip differences of PHA gains, pedestals, and non-linearities. Furthermore, in large SEP events it is important to be able to distinguish hydrogen, helium, and heavier elements on board so that the limited bit rate available to SIS can be devoted primarily to the high-Z, high-energy events which are of greatest interest. This identification requires on-board offset corrections. The offsets, which are measured every 512 seconds and included in the SIS housekeeping data, are subtracted from each event before it is classified according to charge group. The offset-subtracted strip pulse heights are included in the event telemetry, but the original pulse heights can be reconstructed if necessary.

Deviations of the matrix PHAs from linearity were measured using a precision pulser prior to installation in the SIS instrument. Typically we find excellent linearity (few channels) when the VLSI chips are configured for negative input (junction surface of the detector). When used for positive input the integral nonlinearity is a factor ~ 10 larger, but still correctable.

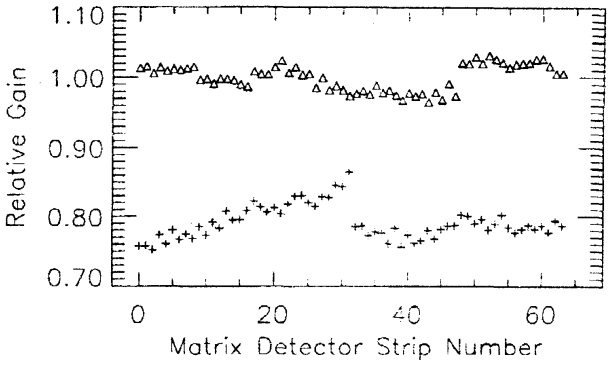

Fig. 3: Relative VLSI gains for all 64 junction surface strips (+) and 64 ohmic surface strips (△) on one matrix detector were derived from measurements with an accelerator beam of ^{56}Fe nuclei. Discontinuities correspond to some of the positions at which adjacent strips are processed by different VLSI chips.

The calibration of the relative gains of the 128 matrix strip PHAs for a particular detector can be readily accomplished using heavy ion data. Since the typical particle produces signals corresponding to the same energy deposition for one strip on each surface of the detector, the ratio of these signals is just the ratio of gains between the two strips (offset corrections having previously been made). A data set either from an accelerator calibration or collected in flight will contain events corresponding to all possible pairs of front-surface/back-surface strips. An iterative procedure can be used to derive all of the strip PHA gains relative to the gain of a selected strip. Figure 3 shows relative gains derived for all the VLSI channels used to read out one matrix detector, based on an accelerator calibration using an ^{56}Fe beam.

ACKNOWLEDGMENTS

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